IN THE CLAIMS

Please cancel claims 1-18 without prejudice.

Please amend the following claims:

1-18. (Canceled)

19. (Original) A method of forming a semiconductor device comprising:

forming a semiconductor body having a top surface and laterally opposite sidewalls on an insulating substrate;

forming a gate dielectric on said top surface of said semiconductor body and on said laterally opposite sidewalls of said semiconductor body;

forming a gate electrode on said gate dielectric and adjacent to said gate dielectric on said laterally opposite sidewalls of said semiconductor body, wherein said gate electrode comprises a metal film formed directly adjacent to said gate dielectric; and

a pair of source/drain regions formed in said semiconductor body on opposite sides of said gate electrode.

20. (Currently Amended) The ~~semiconductor device~~ method of claim 19 wherein said gate electrode comprises only said metal film.

21. (Currently Amended) The ~~semiconductor device~~ method of claim 19 wherein said gate electrode further comprises a doped silicon film formed on said metal film.

22. (Currently Amended) The ~~semiconductor device~~ method of claim 21 wherein said metal film is formed to a thickness between 25-100Å and said doped silicon film is formed to a thickness between 500-3000Å.

23. (Currently Amended) The ~~semiconductor device~~ method of claim 19 wherein in said semiconductor body is silicon, and said source/drain regions have a p type conductivity and said metal film has a work function between 4.9 eV and 5.2 eV.

24. (Currently Amended) The ~~semiconductor device~~ method of claim 19 wherein said semiconductor body is silicon and said source/drain regions have a n type conductivity and said metal film has a workfunction between 3.9 eV and 4.2 eV.

25. (Currently Amended) The ~~semiconductor device~~ method of claim 19 wherein said metal film is selected from a metal having a work function between 4.2 to 4.8 eV.

26. (Currently Amended) The ~~semiconductor device~~ method of claim 19 wherein said gate dielectric is selected from the group consisting of tantalum oxide, titanium oxide, hafnium oxide, zirconium oxide, PZT, BST, aluminum oxide, and silicates thereof.

27. (Original) A method of forming a CMOS integrated circuit comprising:

forming a first and a second semiconductor body on an insulating substrate said first and second semiconductor bodies each having a top surface and a bottom surface and a pair of laterally opposite sidewalls;

forming a first silicon sacrificial gate electrode above said top surface of said first semiconductor body and adjacent to said laterally opposite sidewalls of said semiconductor body, and forming a second silicon sacrificial gate electrode above said top surface of said second semiconductor body and adjacent to said laterally opposite sidewalls of said second semiconductor body;

placing n type dopants into said first silicon sacrificial gate electrode and into said semiconductor body on opposite sides of said first silicon sacrificial gate electrode;

placing p type dopants into said second sacrificial silicon gate electrode and into said second semiconductor body on opposite sides of said second sacrificial gate electrode;

activating said n type and p type dopants so that said n type and p type dopants become substitutional with silicon atoms in said first and second sacrificial silicon gate electrodes;

forming a dielectric layer over said first and second sacrificial gate electrode and over said first and second semiconductor bodies and over said insulating substrate;

planarizing said dielectric layer until the top surface of said dielectric layer is planar with the top surface of said first and second silicon sacrificial gate electrodes and said first and second sacrificial gate electrodes exposed;

removing said first sacrificial gate electrode without removing said second sacrificial gate electrode to form a first opening which exposes the channel region of said first semiconductor body;

forming a gate dielectric layer in said first opening on said top surface and said sidewalls of the channel region of said first semiconductor body;

blanket depositing a first gate electrode material on said gate dielectric layer in said opening on said top surface of said semiconductor body and adjacent to said gate dielectric on said sidewalls of said semiconductor body, wherein said first gate electrode material comprises a first metal film formed directly on and adjacent to said first gate dielectric layer;

removing said first gate electrode material from the top surface of said dielectric film to form a first gate electrode;

removing said second sacrificial gate electrode to form a second opening which exposes the second channel region of said second semiconductor body;

forming a second gate dielectric layer in said second opening on said top surface and sidewalls of said channel region of said second semiconductor body;

blanket depositing a second gate electrode material on said second gate dielectric layer in said second opening on said top surface of said second semiconductor body and adjacent to said second gate dielectric layer on said sidewalls of said semiconductor body, wherein said second gate electrode material comprises a second metal film formed directly on said gate dielectric layer wherein said second metal film is different than said first metal film; and

removing said second gate electrode material from the top surface of said dielectric film to form a second gate electrode.

28. (Original) The method of claim 27 wherein said first and second semiconductor bodies are formed from single crystalline silicon.

29. (Original) The method claim 27 wherein said insulating substrate comprises a lower monocrystalline silicon substrate and a top silicon oxide insulating film.

30. (Original) The method of claim 27 wherein said first metal film is selected from the group consisting of hafnium, zirconium, titanium, tantalum, aluminum, with a workfunction between about 3.9 eV and about 4.2 eV.

31. (Original) The method of claim 27 wherein said second metal film is selected from the group consisting of ruthenium, palladium, platinum, cobalt, nickel, and conductive metal oxides, with a workfunction between about 4.9 eV and 5.2 eV.

32. (Original) The method of claim 27 wherein said first sacrificial gate electrode is removed without masking said second sacrificial gate electrode.

33. (Original) The method of claim 27 wherein said first gate electrode is removed utilizing an etchant selected from the group consisting of ammonium hydroxide and potassium hydroxide.

34. (Original) The method of claim 27 wherein said second sacrificial gate electrode is removed utilizing a wet etchant comprising tetra methyl ammonia hydroxide.

35. (Original) The method of claim 27 further comprising forming a first pair of sidewall spacers adjacent to said laterally opposite sidewalls of said first sacrificial gate electrode and forming a second pair of sidewall spacers adjacent to laterally opposite sidewalls of said second sacrificial gate electrode.

36. (Original) The method of claim 27 further comprising forming silicon on said first and second semiconductor bodies adjacent to said sidewall spacers.

37. (Original) The method of claim 36 further comprising forming silicide on said silicon formed on said first semiconductor body adjacent to said first sidewall spacers and forming silicide on said silicon film formed on said second semiconductor body adjacent to said second sidewall spacers.

38. (Original) A method of forming an integrated circuit comprising:

forming a first sacrificial gate electrode over a channel region of a first semiconductor body and forming a second sacrificial gate electrode over a second channel region of a second semiconductor body;

altering said first sacrificial gate electrode and/or said second sacrificial gate electrode such that said first sacrificial gate electrode can be etched with an etchant without etching said second sacrificial gate electrode;

forming a dielectric layer over said first sacrificial gate electrode, and said second sacrificial gate electrode, and said first semiconductor body and said second semiconductor body;

planarizing said dielectric layer so as to expose said top surface of said first sacrificial gate electrode and said second sacrificial gate electrode;

after altering said first sacrificial gate electrode and/or said second sacrificial gate electrode etching said first sacrificial gate electrode with said etchant without etching said second sacrificial gate electrode to form an opening and expose said channel region of said first semiconductor body;

depositing a first metal film in said opening and over the top of said semiconductor body and adjacent to the sidewalls of said semiconductor body and on the top surface of said dielectric layer;

removing said first metal film from the top of said dielectric layer to form a metal gate electrode;

removing said second sacrificial gate electrode material to form a second opening;

forming a second metal film different than said first metal film over said dielectric layer and into said second opening; and

removing said second metal film from the top surface of said dielectric layer to form a second metal gate electrode.

39. (Original) The semiconductor device of claim 38 wherein first metal film has a work function between 3.9 eV and 4.2 eV.

40. (Original) The method of claim 38 wherein said second metal film has a work function between 4.9 eV to 5.2 eV.

41. (Original) The method of claim 38 wherein said first sacrificial gate electrode and/or said second sacrificial gate electrode are altered by placing dopants therein.

42. (Original) The method of claim 38 wherein both said first and said second sacrificial gate electrode materials are exposed to said etchant.

Pursuant to 37 C.F.R. 1.136(a)(3), applicant(s) hereby request and authorize the U.S. Patent and Trademark Office to (1) treat any concurrent or future reply that requires a petition for extension of time as incorporating a petition for extension of time for the appropriate length of time and (2) charge all required fees, including extension of time fees and fees under 37 C.F.R. 1.16 and 1.17, to Deposit Account No. 02-2666.

Respectfully submitted,

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